CLAIMS

What is claimed is:

1. A circuit for use in a microprocessor, comprising a 4-2 compressor circuit having a full adder formed with dual XOR/XNOR cells and a 2-1 MUX.

2. The circuit according to claim 1 wherein the compressor circuit has a full adder circuit and a XOR/XNOR cell and two pass logic 2-1 multiplexors.

3. The circuit according to claim 2 wherein the XOR/XNOR cell is connected by having input bits X, Y, and Z passed into the full adder, which full adder generates a first order carry out (Cout), an intermediate sum (S), and an intermediate complementary sum (S').

4. The circuit according to claim 3 wherein last input bits (W and Cin) are passed into a second of said dual XOR/XNOR cells generating an intermediate XOR signal (I) and an intermediate XNOR signal (I').

5. The circuit according to claim 4 wherein a complementary sum (S') and an intermediate sum (S)

are passed into one of the 2-1 MUXs using said intermediate XOR signal (I) as the control and wherein the output of said one of the 2-1 MUXs is (10) the final sum (SUM) and said complementary sum (S') and a carry-in bit (Cin) are passed into the final 2-1 MUX.

6. The circuit according to claim 5 wherein said intermediate XNOR is used as the control signal and a (11) second order carry out (Carry) is generated.